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REMARKS

Claim Objections

Claims 1 and 10 are objected to as follows:

In claim 1, "a dielectric layer over the wordline" should be amended to --- an interlayer dielectric layer over the wordline---,

and "the dielectric layer, and a combination thereof." at the end of claim 1 should be amended to --the interlayer dielectric layer, and a combination thereof.--.

In claim 10, "the method of manufacturing an integrated ciruict [sic] as claimed in claim 1" should be amended to --- the method of manufacturing an integrated ciruict [sic] as claimed in claim 6---

With regard to claim 1, line 5, "a dielectric layer over the wordline" has been amended to -- an interlayer dielectric layer over the wordline--. Also, in the last line of claim 5 "the dielectric layer, and a combination thereof." has been amended to --the interlayer dielectric layer, and a combination thereof.--.

With regard to claim 10, line "the method of manufacturing an integrated circuit as claimed in claim 1" has been amended to -- the method of manufacturing an integrated circuit as claimed in claim 6--.

Claim Rejections - 35 USC §102

Claims 1-10 are rejected under 35 USC 102 (e) as being anticipated by Ramkumar et al., U.S. Patent No. 6,677,213 (hereinafter "Ramkumar").

Ramkumar provides a method for processing a semiconductor topography, which includes diffusing deuterium across one or more interfaces of a silicon-oxide-nitride-oxide-silicon (SONOS) structure. In particular, the method may include diffusing deuterium across one or more interfaces of a SONOS structure during a reflow of a dielectric layer spaced above the SONOS structure. In some embodiments, the method may include forming a deutereated nitride layer above the SONOS structure prior to the reflow process. In addition

or alternatively, the method may include forming a deutereated nitride layer within the SONOS structure prior to the reflow process. In some cases, the method may further include annealing the SONOS structure with a deutereated substance prior to forming the deutereated nitride layer. In either embodiment, a SONOS structure may be formed which includes deuterium arranged within an interface of a silicon layer and an oxide layer of the structure.

Regarding claims 1 and 6, Applicants respectfully traverse the rejections since the Applicants' claimed combination, as exemplified in claim 1, includes the limitation not disclosed in Ramkumar of:

"forming first and second bitlines in the semiconductor substrate;"

The Examiner states in the Office Action of 8-10-04 (hereinafter the "Office Action"):

> "Ramkumar et al. discloses the method of forming an integrated circuit (IC) similar to what recited in claim 1. See Figs. 1-8 and Cols. 1-12. The method comprising ... forming first and second bitlines in the substrate (26, Fig. 1)" [deletion for clarity]

However, it is respectfully submitted that Ramkumar does not disclose a method of forming an integrated circuit similar to what is recited in claim 1 in Ramkumar Figs. 1-8 and Cols. 1-12 nor does Ramkumar disclose forming first and second bitlines. Instead Ramkumar discloses manufacturing a SONOS structure as explained in the Ramkumar Abstract and forming source and drain regions in Ramkumar FIG. 1 and col. 7, line 19:

"...including source and drain regions 26."

As well known to those having ordinary skill in the art, Ramkumar is a transistor because of its source and drain regions while the present invention is a memory cell because of its word and bitlines.

Based on the above, it is respectfully submitted Ramkumar does not anticipate claim 1 under 35 USC §102(e) because:

> "Anticipation requires the disclosure in a single prior art reference disclosure of each and every element of the claim under consideration." W.L. Gore & Assocs. v. Garlock, Inc., 721 F.2d 1540, 220 USPQ 303, 313 (Fed. Cir. 1983) (citing Soundscriber Corp. v. United States, 360 F.2d 954, 960, 148 USPQ 298, 301 (Ct. Cl.), *adopted*, 149 USPQ 640 (Ct. Cl. 1966)), *cert. denied*, 469 U.S. 851 (1984). Carella v. Starlight Archery, 804 F.2d 135, 138, 231 USPQ 644, 646 (Fed. Cir.), *modified on reh'g*, 1 USPQ 2d 1209 (Fed. Cir.

1986); RCA Corp. v. Applied Digital Data Sys., Inc., 730 F.2d 1440, 1444, 221 USPQ 385, 388 (Fed. Cir. 1984).

Withdrawal of the rejections is respectfully requested.

Regarding claim 6, this claim has been amended to include the limitation not disclosed in Ramkumar of:

> "forming a spacer around the wordline and on the second dielectric layer;" [underlining for clarity]

Support for the amendment is found in FIG. 5 and in the amended Specification page 8, lines 1-4:

> "The wordline material 515 is patterned, etched, and stripped resulting in wordlines 518 and 519. Spacers 520 and 522 are then formed around the wordlines 518 and 519, respectively, and on the charge trapping dielectric layer 504. A salicide layer is deposited to form salicide areas 524 and 526, respectively, on the tops of the respective wordlines 518 and 519."

Since support for the above amendment is in FIG. 5, no new matter has been introduced by the amendment based on *In re* Wofensperger, 302 F.2d 950, 133 USPQ 537 (CCPA 1962), which held that drawings alone may provide the basis for subsequent amendments to the specification without producing prohibitory new matter.

The Examiner states in the Office Action:

> "Ramkumar et al. discloses the method of forming an integrated circuit (IC) similar to what recited [sic] in claim 6. See Figs. 1-8 and Cols. 1-12. The method comprising ... forming a spacer 24 around the wordline (fig. 1)" [deletion for clarity]

However, it is respectfully submitted that the Applicants' claim limitation is to the spacer being formed over the second dielectric layer, while Ramkumar discloses spacers formed on the substrate and formed around the charge trapping dielectric layer in Ramkumar col. 6, lines 9-14, and FIG. 1:

> "In some embodiments, SONOS structure 28 may further include sidewall spacers 24 as shown in FIG. 1. In general, sidewall spacers 24 may be formed by depositing a dielectric material over SONOS structure 28 and adjacent portions of semiconductor layer 12 using similar techniques as those used for the layers of ONO dielectric 20."

Based on the above, it is respectfully submitted Ramkumar does not anticipate claim 1 under 35 USC §102(e) because:

> "Anticipation requires the disclosure in a single prior art reference disclosure of each and every element of the claim under consideration." W.L. Gore & Assocs. v. Garlock, Inc., 721 F.2d 1540, 220 USPQ 303, 313 (Fed. Cir. 1983) (citing Soundscriber Corp. v. United States, 360 F.2d 954, 960, 148 USPQ 298, 301 (Ct. Cl.), *adopted*, 149 USPQ 640 (Ct. Cl. 1966)), *cert. denied*, 469 U.S. 851 (1984). Carella v. Starlight Archery, 804 F.2d 135, 138, 231 USPQ 644, 646 (Fed. Cir.), *modified on reh'g*, 1 USPQ 2d 1209 (Fed. Cir. 1986); RCA Corp. v. Applied Digital Data Sys., Inc., 730 F.2d 1440, 1444, 221 USPQ 385, 388 (Fed. Cir. 1984).

Withdrawal of the rejections is respectfully requested.

Regarding claims 2-5, and 7-10, these dependent claims depend from independent claims 1 and 6 and are believed to be allowable since they contain all the limitations set forth in the independent claims from which they depend and claim additional unobvious combinations thereof.

Withdrawal of the rejections is respectfully requested.

Other

Applicants have updated the Cross-Reference to Related Applications section to indicate that U.S. Application No. 10/128,771 has now issued as U.S. Patent No. 6,670,241 B1 and is incorporated by reference.

Conclusion

In view of the above, it is submitted that the claims are in condition for allowance and reconsideration of the rejections is respectfully requested. Allowance of claims 1-10 at an early date is solicited.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this

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paper, including any extension of time fees, to Deposit Account No. 01-0365 and please credit any excess fees to such deposit account.

Respectfully submitted,

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